CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

The compact design of the control PWB is obtained by using Risc Processor (CPU) in the main control section and high density printing of surface mounting parts. Each PWB is independent according to its function as shown in Fig. 1.

2. PWB configuration

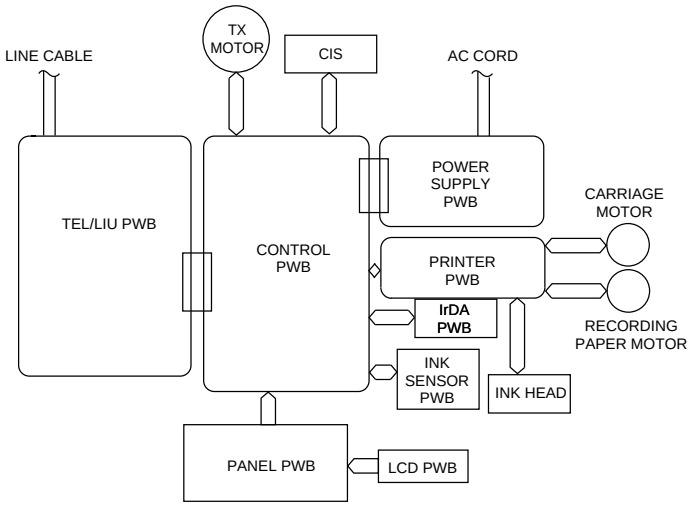

Fig. 1

1) Control PWB

The control PWB controls peripheral PWBs, mechanical parts, transmission, and performs overall control of the unit.
This machine employs a 1-chip modem (R144AFXL) which is in-stalled on the control PWB.

2) TEL/LIU PWB

This PWB controls connection of the telephone line to the unit.

3) Power supply PWB

This PWB provides voltages of +5V, VREG and +24V to the another PWB.

4) Panel PWB

The panel PWB allows input of the operation keys.

5) Printer PWB

This PWB controls the printer mechanical parts.
This PWB employs 8bit CPU that is installed on printer PWB.
This CPU control a printer mechanical parts.

6) LCD PWB

This PWB controls the LCD display.

7) IrDA PWB

This PWB employs led and sensor.

8)Ink sensor PWB

This PWB examine the ink level of the cartridge.

3. Operational description

Operational descriptions are given below:

- Transmission operation

  When a document is loaded in standby mode, the state of the document sensor is sensed via the CPU (SH2).
  If the sensor signal was on, the motor is started to bring the document into the standby position. With depression of the START key in the off-hook state, transmission takes place.

  Then, the procedure is sent out from the modem and the motor is rotated to move the document down to the scan line. In the scan processor, the signal scanned by the CIS is sent to the internal image processor and the AD converter to convert the analog signal into binary data. This binary data is transferred from the scan processor to the image buffer within the RAM and encoded and stored in the transmit buffer of the RAM. The data is then con-verted from parallel to serial form by the modem where the serial data is modulated and sent onto the line.

- Receive operation

  There are two ways of starting reception, manual and automatic.
  Depression of the START key in the off-hook mode in the case of manual receive mode, or CI signal detection by the LIU in the automatic receive mode.

  First, the CPU(SH2) controls the procedure signals from the modem to be ready to receive data. When the program goes into phase C, the serial data from the modem is converted to parallel form in the modem interface of the 1 fax CPU(SH2) which is stored in the receive buffer of the RAM. The data in the receive buffer is decoded software-wise to reproduce it as binary image data in the image buffer. The data is DMA transferred to the recording processor within the printer control gate array which is on printer PWB and sent to the ink head. The data is printed by printer gate arrey and fine signal.

- Copy operation

  To make a copy on this facsimile, the COPY key is pressed when the machine is in stand-by with a document on the document table and the telephone set is in the on-hook state.

  First, depression of the COPY key advances the document to the scan line. Similar to the transmitting operation, the image signal from the CIS is converted to a binary signal in the DMA mode via the reading processor which is then sent to the image buffer of the RAM. Next, the data is transferred to the recording processor in the DMA mode to send the image data to the ink head which is printed swath by swath. The copying takes place as the operation is repeated.

[2] Circuit description of control PWB

1. General description

Fig. 2 shows the functional blocks of the control PWB, which is composed of 5 blocks.

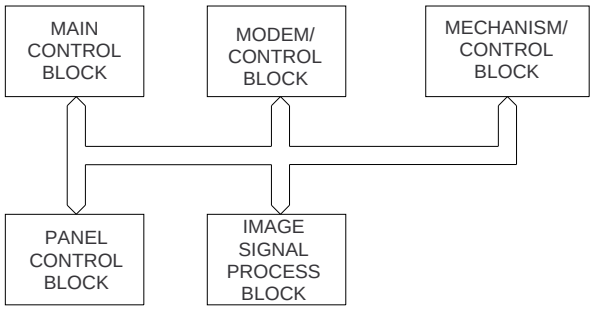

Fig. 2 Control PWB functional block diagram

2. Description of each block

(1) Main control block

The main control block is composed of HITACHI CPU (SH2), ROMX2 (256KByte), RAMX2 (32KByte), DRAMX2 (512KByte). Devices are connected to the bus to control the whole unit.

1) SH7040 (IC12) : pin-112 QFP (SH7040)

The CPU Integrated Facsimile Controllers.

SH7040(SH2), contains an internal 32 bit microprocessor with an external 16 bit address space and dedicated circuitry optimized for facsimile image processing and facsimile machine control and monitoring.

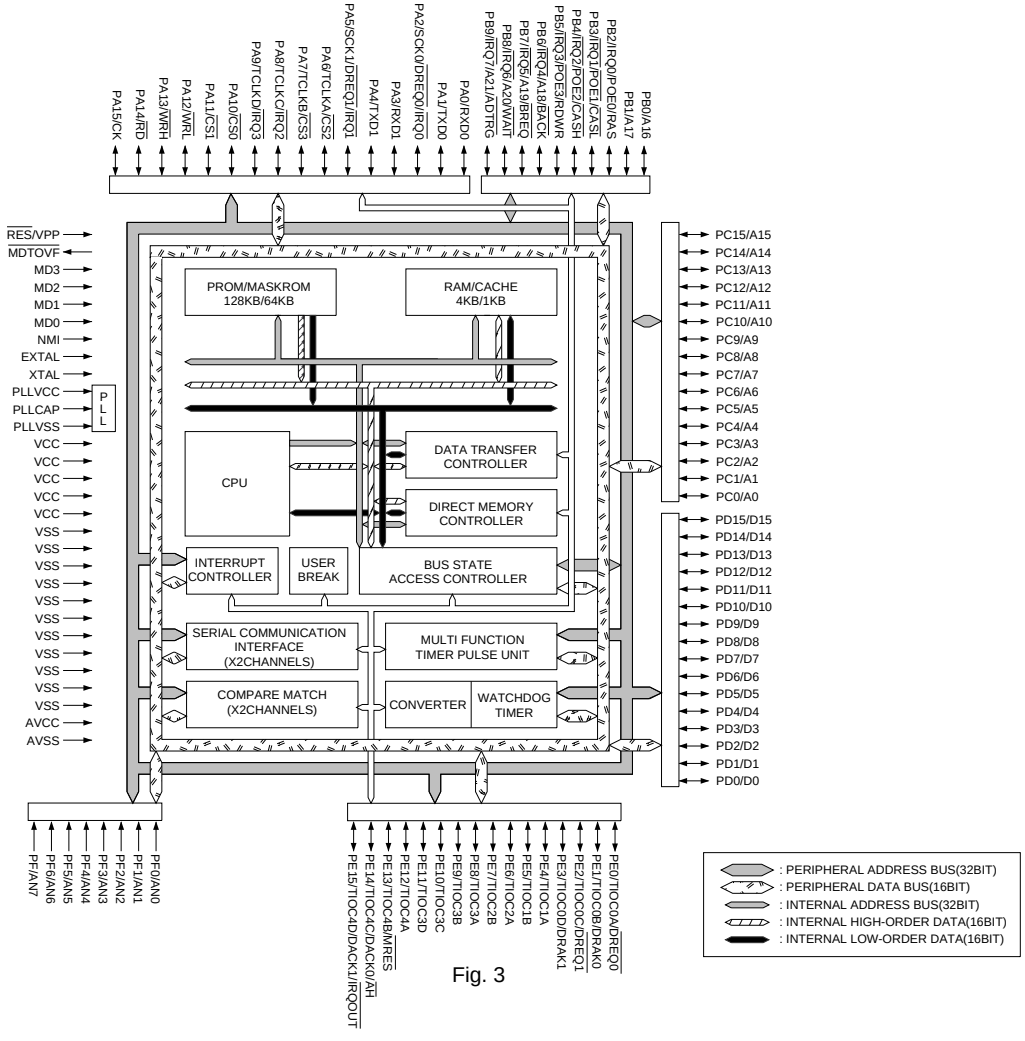

Fig. 3

2) M27C4001 (IC18, IC19): pin-32 DIP (ROM)

EPROM of 2Mbit equipped with software for the main CPU.

3) SRM2B257SLMX70 (IC17, IC24): pin-28 SOP (RAM)

Line memory for the main CPU system RAM area and coding/decoding process. Used as the transmission buffer.

Memory of recorded data such as daily report and auto dials. When the power is turned off, this memory is backed up by the lithium battery.

4) MSM514800 (IC16, IC23): pin-28 SOJ (RAM)

Image memory for recording process.

- Memory for recording pixel data at without paper.

SH7040 (IC12) Terminal list

QFP112 Pin No.	MCU MODE	PROM MODE
1	PE14/TIOC4C/DACK0/$\overline{AH}$	VCC
2	PE15/TIOC4D/DACK1/$\overline{IRQOUT}$	$\overline{CE}$
3	VSS	VSS
4	PC0/A0	A0
5	PC1/A1	A1
6	PC2/A2	A2
7	PC3/A3	A3
8	PC4/A4	A4
9	PC5/A5	A5
10	PC6/A6	A6
11	PC7/A7	A7
12	PC8/A8	A8
13	PC9/A9	N.C.
14	PC10/A10	A10
15	PC11/A11	A11
16	PC12/A12	A12
17	PC13/A13	A13
18	PC14/A14	A14
19	PC15/A15	A15
20	PB0/A16	A16
21	VCC	VCC
22	PB1/A17	N.C.
23	VSS	VSS
24	PB2/$\overline{IRQ0}$/$\overline{POE0}$/$\overline{RAS}$	N.C.
25	PB3/$\overline{IRQ1}$/$\overline{POE1}$/$\overline{CASL}$	$\overline{OE}$
26	PB4/$\overline{IRQ2}$/$\overline{POE2}$/$\overline{CASH}$	$\overline{PGM}$
27	VSS	VSS
28	PB5/$\overline{IRQ3}$/$\overline{POE3}$/RDWR	VCC
29	PB6/$\overline{IRQ4}$/A18/$\overline{BACK}$	N.C.
30	PB7/$\overline{IRQ5}$/A19/$\overline{BREQ}$	N.C.
31	PB8/$\overline{IRQ6}$/A20/$\overline{WAIT}$	N.C.
32	PB9/$\overline{IRQ7}$/A21/$\overline{ADTRG}$	N.C.
33	VSS	VSS
34	PA14/$\overline{RD}$	N.C.
35	$\overline{WDTOVF}$	N.C.
36	PA13/$\overline{WRH}$	N.C.
37	VCC	VCC
38	PA12/$\overline{WRL}$	N.C.
39	VSS	VSS
40	PA11/$\overline{CS1}$	N.C.
41	PA10/$\overline{CS0}$	N.C.
42	PA9/TCLKD/$\overline{IRQ3}$	N.C.
43	PA8/TCLKC/$\overline{IRQ2}$	N.C.
44	PA7/TCLKB/$\overline{CS3}$	N.C.
45	PA6/TCLKA/$\overline{CS2}$	N.C.
46	PA5/SCK1/$\overline{DREQ1}$/$\overline{IRQ1}$	N.C.
47	PA4/TXD1	N.C.
48	PA3/RXD1	N.C.
49	PA2/SCK0/$\overline{DREQ0}$/$\overline{IRQ0}$	N.C.
50	PA1/TXD0	N.C.
51	PA0/RXD0	N.C.
52	PD15/D15	N.C.
53	PD14/D14	N.C.
54	PD13/D13	N.C.
55	VSS	VSS
56	PD12/D12	N.C.
57	PD11/D11	N.C.
58	PD10/D10	N.C.
59	PD9/D9	N.C.

Pin No.	MCU MODE	PROM MODE
60	PD8/D8	N.C.
61	VSS	VSS
62	PD7/D7	D7
63	PD6/D6	D6
64	PD5/D5	D5
65	VCC	VCC
66	PD4/D4	D4
67	PD3/D3	D3
68	PD2/D2	D2
69	PD1/D1	D1
70	PD0/D0	D0
71	VSS	VSS
72	XTAL	N.C.
73	MD3	VCC
74	EXTAL	VSS
75	MD2	VCC
76	NMI	A9
77	VCC	VCC
78	MD1	VCC
79	MD0	VCC
80	PLLVCC	VCC
81	PLLCAP	VSS
82	PLLVSS	VSS
83	PA15/CK	N.C.
84	$\overline{RES}$	VPP
85	PE0/TIOC0A/$\overline{DREQ0}$	N.C.
86	PE1/TIOC0B/DRAK0	N.C.
87	PE2/TIOC0C/$\overline{DREQ1}$	N.C.
88	PE3/TIOC0D/DRAK1	N.C.
89	PE4/TIOC1A	N.C.
90	VSS	VSS
91	PF0/AN0	VSS
92	PF1/AN1	VSS
93	PF2/AN2	VSS
94	PF3/AN3	VSS
95	PF4/AN4	VSS
96	PF5/AN5	VSS
97	AVSS	VSS
98	PF6/AN6	VSS
99	PF7/AN7	VSS
100	AVCC	VCC
101	VSS	VSS
102	PE5/TIOC1B	N.C.
103	VCC	VCC
104	PE6/TIOC2A	N.C.
105	PE7/TIOC2B	N.C.
106	PE8/TIOC3A	N.C.
107	PE9/TIOC3B	N.C.
108	PE10/TIOC3C	N.C.
109	VSS	VSS
110	PE11/TIOC3D	N.C.
111	PE12/TIOC4A	N.C.
112	PE13/TIOC4B/$\overline{MRES}$	N.C.

SH7040 (IC12) Terminal function

Classification	Symbol	Input/Output	Name	Function
Power	Vcc	Input	Power	Connect the Vcc terminal to the power of all systems. Operation is not performed if there is open terminal.
	Vss	Input	Ground	Connect to the ground. Connect the Vss terminal to the ground of all systems. Operation is not performed if there is open terminal.
	Vpp	Input	Program power	In case of normal operation connect to the power (Vcc). In the PROM mode 12.5V is applied.
Clock	PLLVcc	Input	Power for PLL	Power for built-in PLL oscillator.
	PLLVss	Input	Ground for PLL	Ground for built-in PLL oscillator.
	PLLCAP	Input	Capacity for PLL	Externally provided capacity terminal for built-in PLL oscillator.
	EXTAL	Input	External clock	Connect the crystal oscillator. It is possible to input also the external clock to the EXTAL terminal.
	EXTAL	Input	Crystal	Connect the crystal oscillator.
	CK	Output	System clock	The system clock is supplied to the peripheral device.
System control	$\overline{\text{RES}}$	Input	Power-on reset	When Low Level is applied to this terminal, power-on reset state is generated.
	$\overline{\text{MRES}}$	Input	Manual reset	When Low Level is applied to this terminal, the manual reset state is generated.
	$\overline{\text{WDTOVF}}$	Output	Watch dog timer overflow	Overflow output signal from WDT.
	$\overline{\text{BREQ}}$	Input	Bus right request	Low level is generated when the external device requestes release of bus right.
	$\overline{\text{BACK}}$	Output	Bus right request acknowledge	It is indicated that the bus right has been released for the external device. The device whitch output the BREQ signal receives the BACK signal, thereby allowing to know that the bus right has been obtained.
Operation mode control	MD0 ~ MD3	Input	Mode setting	Terminal to decide the operation mode. During operation do not change the input value.
Interruption	NMI	Input	Nonmaskable interruption	Nonmaskable interruption request terminal. It is possible to select reception at rise edge or fall edge.
	$\overline{\text{IRQ0}}$ ~ $\overline{\text{IRQ7}}$	Input	Interruption request 0 to 7	Maskable interruption request terminal. It is possible to select level input and edge input.
	$\overline{\text{IRQOUT}}$	Output	Interruption request output	Indicates occurrence of interruption factor. Occurrence of interruption can be known also during bus release.
Address bus	A0 ~ A21	Output	Address bus	Address is output.
Data bus	D0 ~ D15 (QFP-112) D0 ~ D31 (QFP-144)	Output	Data bus	16-bit (QFP-112 pin type) or 32-bit (QFP-144 pin type) two-direction data bus.
Bus control	$\overline{\text{CS0}}$ ~ $\overline{\text{CS3}}$	Output	Chip selection 0 to 3	Chip selection signal for external memory or device.
	$\overline{\text{RD}}$	Output	Reading	Indicates reading from the external device.
	$\overline{\text{WRH}}$	Output	High-order side writing	Indicates writing into high-order 8 bits (bit 15 to 8) of external data.
	$\overline{\text{WRL}}$	Output	Low-order side writing	Indicates writing into Low-order 8 bits (bit 7 to 0) of external data.
	$\overline{\text{WAIT}}$	Input	Wight	Input to insert the weight cycle into bus cycle when access to the external space is made.
	$\overline{\text{RAS}}$	Output	Low address strobe	Dram low address strobe timing signal.

SH7040 (IC12) Terminal function

Classification	Symbol	Input/Output	Name	Function
Bus control	$\overline{CASH}$	Output	High-order column address strobe	DRAM column address strobe timing signal. It is output when access to high-order 8bits of data is made.
	$\overline{CASL}$	Output	Low order column address strobe	DRAM column address strobe timing signal.
	RDWR	Output	Dram reading/writing	DRAM writing strobe signal.
	$\overline{AH}$	Output	Address hold	Address hold timing signal for the device which used address/data multiplex bus.
	$\overline{WRHH}$(QFP-144)	Output	HHside writting	Indicates that bit 24 is written from bit 31 of external data.
	$\overline{WRHL}$(QFP-144)	Output	HLside writting	Indicates that bit 15 is written from bit 23 of external data.
	$\overline{CASHH}$(QFP-144)	Output	HH side column address strobe	DRAM column address strobe timing signal. It is output when access to bit 24 from bit 31 of data is made.
	$\overline{CASHL}$(QFP-144)	Output	HL side column address strobe	DRAM column address strobe timing signal. It is output when access to bit 16 from bit 23 of data is made.
Multifunction timer pulse unit	TCLKA TCLKB TCLKC TCLKD	Input	MTU timer clock input	MTU counter external clock input terminal.
	TIOC0A TIOC0B TIOC0C TIOC0D	Input/output	MTU input capture/ output conveyer (channel 0)	Channel 0 input capture input/output conveyer output/PWM output terminal.
	TIOC1A TIOC1B	Input/output	MTU input capture/ output conveyer (channel 1)	Channel 1 input capture input/output conveyer output/PWM output terminal.
	TIOC2A TIOC2B	Input/output	MTU input capture/ output conveyer (channel 2)	Channel 2 input capture input/output conveyer output/PWM output terminal.
	TIOC1A TIOC1B	Input/output	MTU input capture/ output conveyer (channel 3)	Channel 3 input capture input/output conveyer output/PWM output terminal.
	TIOC1A TIOC1B	Input/output	MTU input capture/ output conveyer (channel 4)	Channel 4 input capture input/output conveyer output/PWM output terminal.
Direct memory access controller (DMAC)	DREQ0 DREQ1	Input	DMA transfer request (channel 0,1)	From-external DMA transfer request input terminal.
	DRAK0 DRAK1	Output	DREQ request reception (channel 0,1)	From-external DMA transfer request input sampling reception is output.
	DACK0 DACK1	Output	DMA transfer strobe (channel 0,1)	From-external DMA transfer request external I/O strobe is output.
Serial communication interface (SCI)	TxD0 TxD1	Output	Transmission data (channel 0 to 1)	SCI 0 and 1 transmission data output terminal.
	RxD0 RxD1	Input	Reception data (channel 0 to 1)	SCI 0 and 1 reception data input terminal.
	SCK0 SCK1	Input/output	Serial clock (channel 0 to 1)	SCI 0 and 1 clock input/output terminal.
A.D converter	AVcc	Input	Analog power	Analog power Vcc potential is connected.
	AVss	Input	Analog ground	Analog power Vss potential is connected.
	AVref (QFP-144)	Input	Analog reference power	Analog reference power input terminal.
	AN0 ~ AN7	Input	Analog input	Analog signal input terminal.
	ADTRG	Input	A/D conversion trigger input	A/D conversion state external trigger input.

SH7040 (IC12) Terminal function

Classification	Symbol	Input/Output	Name	Function
I/O port	POE0 ~ POE3	Input	Port output enable	Input terminal to perform port terminal drive control when the general-use port is set to output.
	PA0 ~ PA15 (QFP-112) PA0 ~ PA23 (QFP-144)	Input/output	General use port	General-use input/output port terminal. It is possible to specify input/output for each bit.
	PB0 ~ PB9	Input/output	General use port	General-use input/output port terminal. It is possible to specify input/output for each bit.
	PC0 ~ PC15	Input/output	General use port	General-use input/output port terminal. It is possible to specify input/output for each bit.
	PD0 ~ PD15 (QFP-112) PD0 ~ PD31 (QFP-144)	Input/output	General use port	General-use input/output port terminal. It is possible to specify input/output for each bit.
	PE0 ~ PE15	Input/output	General use port	General-use input/output port terminal. It is possible to specify input/output for each bit.
	PF0 ~ PF7	Input	General use port	General-use input port terminal.

(2) Panel control block

The following controls are performed by the Gate array (LZ9FJ49).

- Operation panel key scanning
- Operation panel LCD display

(3) Mechanism/recording control block

The following controls are performed by Gate array (LZ9FJ49).

- TX Motor control

The following controls are performed by CPU (SH2).

- Sensor detection

The following controls are performed by Gate array (TC160G33:PRINTER PWB).

- Carrier Motor control
- Feed Motor control

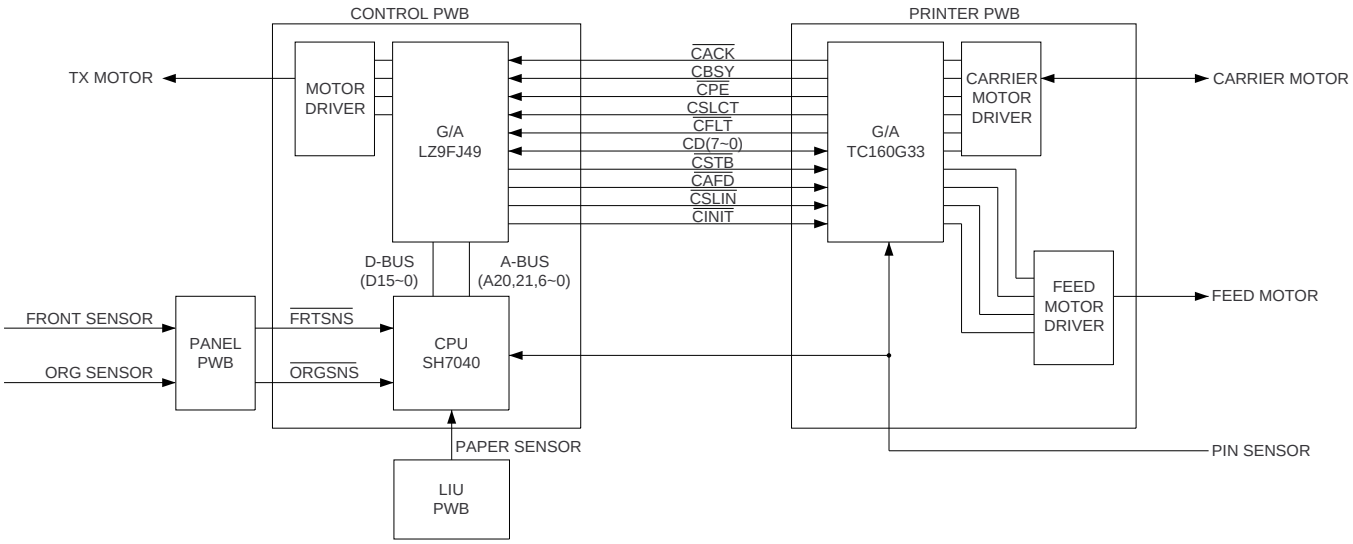

Fig. 4

(4) Modem (R144EFXL) block

INTRODUCTION

The Rockwell R144EFXL MONOFAX modem is a synchronous 14400 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires only a single +5V DC power supply. The modem is housed in a single VLSI device package.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The R144EFXL is designed for use in Group 3 facsimile ma-chines.

The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2 and T.4, and meets the binary signaling requirements of T.30.

The modem can operate at 14400, 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 ter short training sequence option.

The modem can also perform HDLC framing according to T.30 at 14400, 9600, 7200, 4800, 2400, or 300 bps.

The modem features a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 receiver.

The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.

The modem is available in either a 100-pin plastic quad flat pack (PQFP) or a 64-pin quad in-line package (QUIP).

General purpose input/output (GPIO) pins are available for host as signment in the 100-pin PQFP.

The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.

MONOFAX is a registered trademark of Rockwell International.

FEATURES

- Group 3 facsimile transmission/reception
  - – ITU-TS V.29, V.27 ter, T.30, V.21 Channel 2, T.4
  - – HDLC Framing at all speeds
- V.27 ter short train
- Concurrent DTMF, FSK, and tone reception
- Voice mode transmission/reception
- Half-duplex (2-wire)
- Programmable maximum transmit level:
  - 0 dBm to –15 dBm
- Programmable transmit analog attenuation:
  - 0 dB to 14 dB in 2 dB steps
- Receive dynamic range: 0 dBm to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - – Allows telephone line quality monitoring
- Equalization
  - – Automatic adaptive equalizer
  - – Fixed digital compromise equalizer
- DTE interface: two alternate ports
  - – Selectable microprocessor bus (6500 or 8085)
  - – CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption: 275 mW (typical)
- Single Package
  - – 100-pin PQFP
  - – 64-pin QUIP
- Single +5VDC power supply

R96DFXL-CID (IC11) Hardware Interface Signals

Pin No.	Signal Name	I/O Type
1	GP03	IA/OB
2	GP04	IA/OB
3	GP05	IA/OB
4	GP06	IA/OB
5	GP07	IA/OB
6	0VD2	GND
7	0VD2	GND
8	D7	IA/OB
9	D6	IA/OB
10	D5	IA/OB
11	D4	IA/OB
12	D3	IA/OB
13	D2	IA/OB
14	D1	IA/OB
15	D0	IA/OB
16	0VD2	GND
17	0VA	GND
18	RAMPIN	R
19	NC	
20	NC	
21	0VA	GND
22	+5VD2	PWR
23	0VD1	GND
24	SWGAINI	R
25	ECLKIN1	R
26	SYNCIN1	R
27	NC	
28	NC	
29	NC	
30	0VA	GND
31	NC	
32	NC	
33	NC	
34	DAIN	R
35	ADOUT	R
36	BYPASS	IC
37	RCVI	R
38	TXLOSS3	IC
39	TXLOSS2	IC
40	TXLOSS1	IC
41	NC	
42	NC	
43	0VA	GND
44	TXOUT	AA
45	RXIN	AB
46	+5VA	PWR
47	0VA	GND
48	AGD	R
49	AOUT	R
50	0VD1	GND
51	NC	
52	$\overline{\text{IRQ}}$	OC
53	$\overline{\text{WRITE}}$-R/$\overline{\text{W}}$	IA
54	$\overline{\text{CS}}$	IA
55	$\overline{\text{READ}}$-ϕ2	IA
56	RS4	IA
57	RS3	IA
58	RS2	IA
59	RS1	IA

Pin No.	Signal Name	I/O Type
60	RS0	IA
61	GP13	IA/OB
62	NC	
63	GP11	IA/OB
64	$\overline{\text{RTS}}$	IA
65	$\overline{\text{EN85}}$	R
66	0VD2	GND
67	$\overline{\text{PORI}}$	ID
68	XTLI	R
69	XTLO	R
70	XCLK	OD
71	YCLK	OD
72	+5VD1	PWR
73	DCLK1	R
74	SYNCIN2	R
75	GP16	IA/OB
76	GP17	IA/OB
77	0VD2	GND
78	$\overline{\text{CTS}}$	OA
79	TXD	IA
80	0VD2	GND
81	0VD2	GND
82	DCLK	OA
83	EYESYNC	OA
84	EYECLKX	OA
85	EYECLK	OA
86	EYEX	OA
87	ADIN	R
88	DAOUT	R
89	0VD2	GND
90	EYEY	OA
91	GP21	IA/OB
92	0VD2	GND
93	GP20	IA/OB
94	GP19	IA/OB
95	RXD	OA
96	$\overline{\text{RLSD}}$	OA
97	0VD2	GND
98	RCVO	R
99	SWGAINO	R
100	GP02	IA/OB

Notes:
1. NC = No connection; leave pin disconnected (open).
2. I/O Type: = Digital signals: see Table 9;
   Analog signals: see Table 10.
3. R = Required modem inter-connection; no connection to host equipment.

(5) Image signal process block

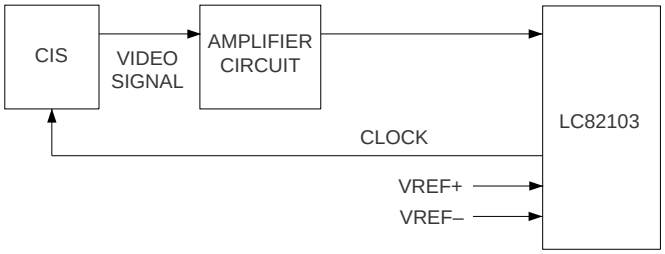

Fig. 5

The CIS is driven by the LSI (LC82103), and the output video signal from the CIS is input into the LC82103 through the amplifying circuit . The ADC and buffer are provided in the LC82103, and the digital image processing is performed.

(6) Speaker amplifier

The speaker amplifier monitors the line under the on-hook mode, outputs the buzzer sound generated from the SH7040, ringer sound, DTMF generated from the modem, and line sound.

(7) Adjustment of voice/ringer volume

The voice/ringer volume can be adjusted by using the panel bottons "UP" and "DOWN".

- The ringer volume can be adjusted in the Stand-by mode by pressing the UP/DOWN button.
- The reception level can be adjusted by pressing the UP/DOWN button when the handset is located in the off-hook state.
- The speaker volume can be adjusted by using the speaker key.

[3] Circuit description of TEL/LIU PWB

(1) TEL/LIU block operational description

1) Block diagram

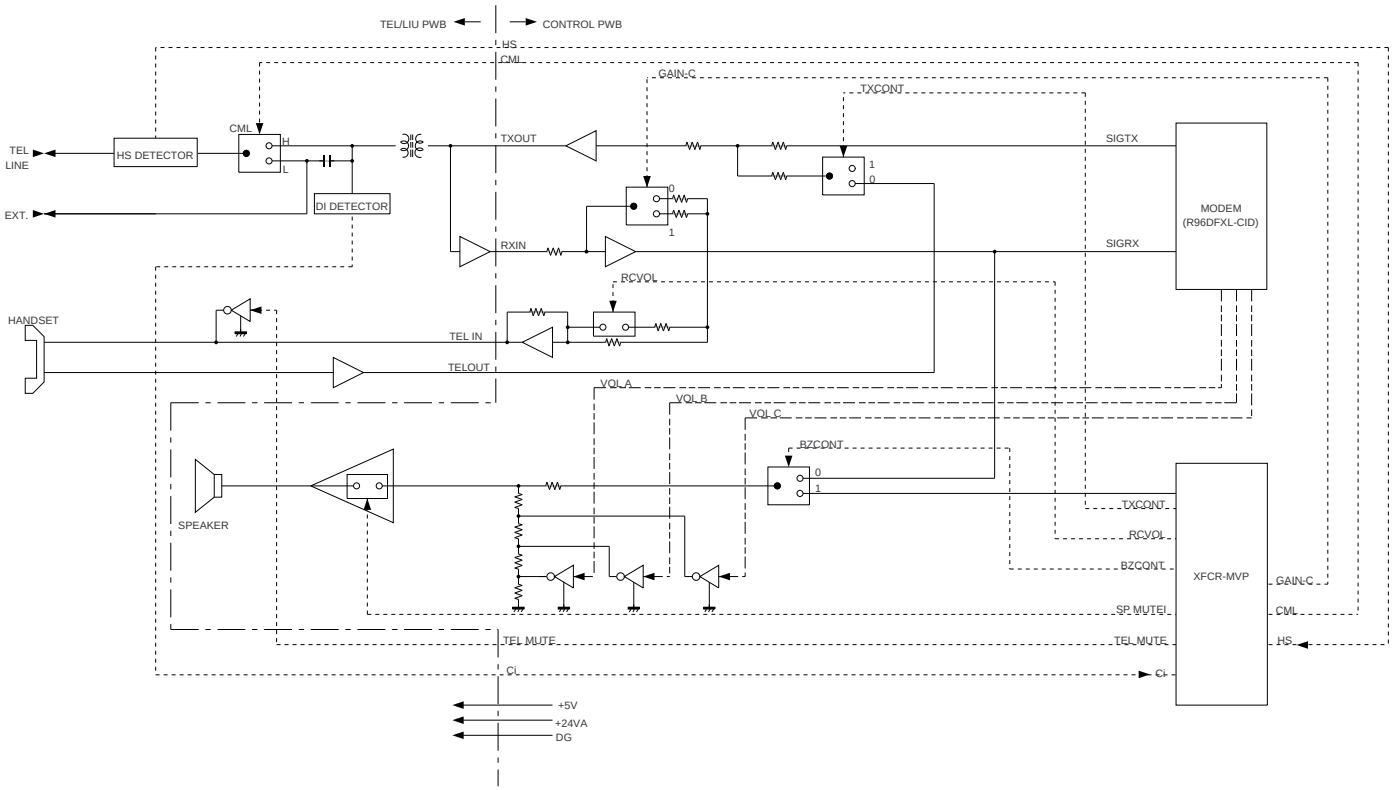

Fig. 6

2) Circuit description

The TEL/LIU PWB is composed of the following 10 blocks.

1. Surge protection circuit
2. On-hook status detection circuit
3. Dial pulse generation circuit
4. CML relay
5. Matching transformer
6. Hybrid circuit
7. Signal selection
8. Sensor circuit
9. Cl detection circuit
10. Power supply and bias circuit

3) Block description

1. Surge Protection circuit

This circuit protects the circuit from the surge voltage occurring on the telephone line.

- The AR1 protects the circuit from the 390V or higher line surge voltages.
- The VA1 and VA2 protect the circuit from the 470V or higher vertical surge voltages.

2. On-hook status detection circuit

The on-hook status detection circuit detects the Status of the hook switch (RHS) of Built-in telephone, and the status of the hook of a telephone externally connected.

- The status of on-hook switch (RHS) is determined from the logical level of $\overline{\text{RHS}}$ signal.

  $\overline{\text{RHS}}$ LOW : ON-HOOK

  $\overline{\text{RHS}}$ HIGH : OFF-HOOK

- External telephone hook status detection circuit ($\overline{\text{HS1}}$)

This circuit comprises the photo-coupler PC1, resistors R3 and R4, Zener diodes ZD1 and ZD2.

When an external telephone is connected and enters the on-hook mode, the LED of photo-coupler PC1 emits light and the light receiv ing element turns on. The status signal $\overline{\text{HS1}}$ is input to the pin 84 of (XFCR-MVP) (IC4: control PWB).

$\overline{\text{HS1}}$ LOW : EXT. TEL OFF-HOOK

$\overline{\text{HS1}}$ HIGH : EXT. TEL ON-HOOK

3. Dial pulse generation circuit

The pulse dial generation circuit comprises the CML relay.

4. CML relay

The CML relay switches over connection to the matching transformer T1 while the FAX or built-in telephone is being used.

5. Matching transformer

The matching transformer performs electrical insulation from the telephone line and impedance matching for transmitting the TEL/FAX signal.

6. Hybrid circuit

The hybrid circuit performs 2-wire-to-4-wire conversion using the IC2 of operational amplifier, transmits the voice transmission signal to the line, and feeds back the voice signal to the voice reception circuit as the side tone.

7. Signal selection

The following signals are used to control the transmission line of TEL/FAX signal. For details, refer to the signal selector matrix table.

[Control signals from output port]

<table>
<tr><th>Signal Name</th><th>Description</th></tr>
<tr><td>CML</td><td>Line connecting relay and DP generating relay
H: Line make
L: Line break</td></tr>
<tr><td>SP MUTE</td><td>Speaker tone mute control signal
H: Muting (Power down mode)
L: Muting cancel (Normal operation)</td></tr>
<tr><td>TEL MUTE</td><td>Handset reception mute control signal
H: Muting
L: Muting cancel</td></tr>
<tr><td>RCVOL

(The circuit is located in the control PWB.)</td><td>Handset receiver volume control signal
<table>
<tr><th>Volume</th><th>High</th><th>Middle</th><th>DTMF sending</th></tr>
<tr><td>RCVOL</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>
SIDE KICK is two-stage switching.
Note: The DTMF sending listed above is DTMF signal sending in the handset OFF-HOOK mode.</td></tr>
<tr><td>VOL A
VOL B
VOL C

(The circuit is located in the control PWB.)</td><td>Speaker volume control signal
VRSEL1 VRSEL2 matrix
<table>
<tr><th></th><th>VOL A</th><th>VOL B</th><th>VOL C</th><th>RING./ Receiving</th><th>Buzzer</th><th>DTMF</th></tr>
<tr><td></td><td>L</td><td>L</td><td>L</td><td>High</td><td>—</td><td>High</td></tr>
<tr><td></td><td>H</td><td>L</td><td>L</td><td>Middle</td><td>Fixed</td><td>Middle</td></tr>
<tr><td></td><td>L</td><td>L</td><td>H</td><td>Low</td><td>—</td><td>Low</td></tr>
</table></td></tr>
<tr><td>TXCONT
(The circuit is located in the control PWB.)</td><td>TXOUT mute signal
H: Signal sending, when transmitting
L: During reception, transmission mute, (during standby)</td></tr>
<tr><td>GAIN-C
(The circuit is located in the control PWB.)</td><td>Reception gain switching signal
L: When connected to line, 1: 1 gain
H: When not connected to line, HIGH gain</td></tr>
<tr><td>MPX A
(The circuit is located in the control PWB.)</td><td>Transmission/transfer switching signal
H: When transmitting modem signal (during standby)
L: When transferring</td></tr>
<tr><td>BZCONT
(The circuit is located in the control PWB.)</td><td>Speaker output signal switching
H: Buzzer signal output
L: When monitoring line signal</td></tr>
</table>

[Signals for status recognition according to input signals]

Signal Name	Function
$\overline{\text{RHS}}$	H: The handset is in the on-hook state. L: The handset is in the off-hook state.
CI	Incoming call (CI) detection signal.
$\overline{\text{HS}}$	H: The handset or external telephone is in the on-hook state. L: The handset or external telephone is in the off-hook state.
P.E	L: No recording paper. H: Recording paper exists.
DRSNS	H: Door open. L: Door close.

[Other signals]

Signal Name	Function
TEL IN	Receiving signal from line or modem
TEL OUT	Transfer signal to line
TXOUT	Transmission (DTMF) analog signal output from modem
RXIN	Reception (DTMF, others) analog signal input into modem

NO	Signal Name (CNLIU)	NO	Signal Name (CNLIU)
1	+24VA	8	RHS
2	DG	9	TXOUT
3	$\overline{\text{PE}}$	10	RXIN
4	+5V	11	TELMUTE
5	CML	12	N.C.
6	CI	13	TELOUT
7	HS	14	TELIN

8. Sensor circuit

For the recording paper sensor (P.E), when there is recording paper, the photo transistor in the light receiving side is ON and the detection level is LOW. When there is no recording paper, the photo transistor in the light receiving side is OFF and the detection level is HIGH.

9. CI detection circuit

The CI detection circuit detects the CI signals of 15.3Hz to 68Hz.
A CI signal, which is provided to the photo-coupler PC1 through the C1 (0.82 uF), R3 (22 K), and ZD3 when the ring signal is inputted from the telephone line.

10. Power supply and bias circuits

The voltages of +5V and +24VA are supplied from the control PWB unit.

(Example: Fax signal send)

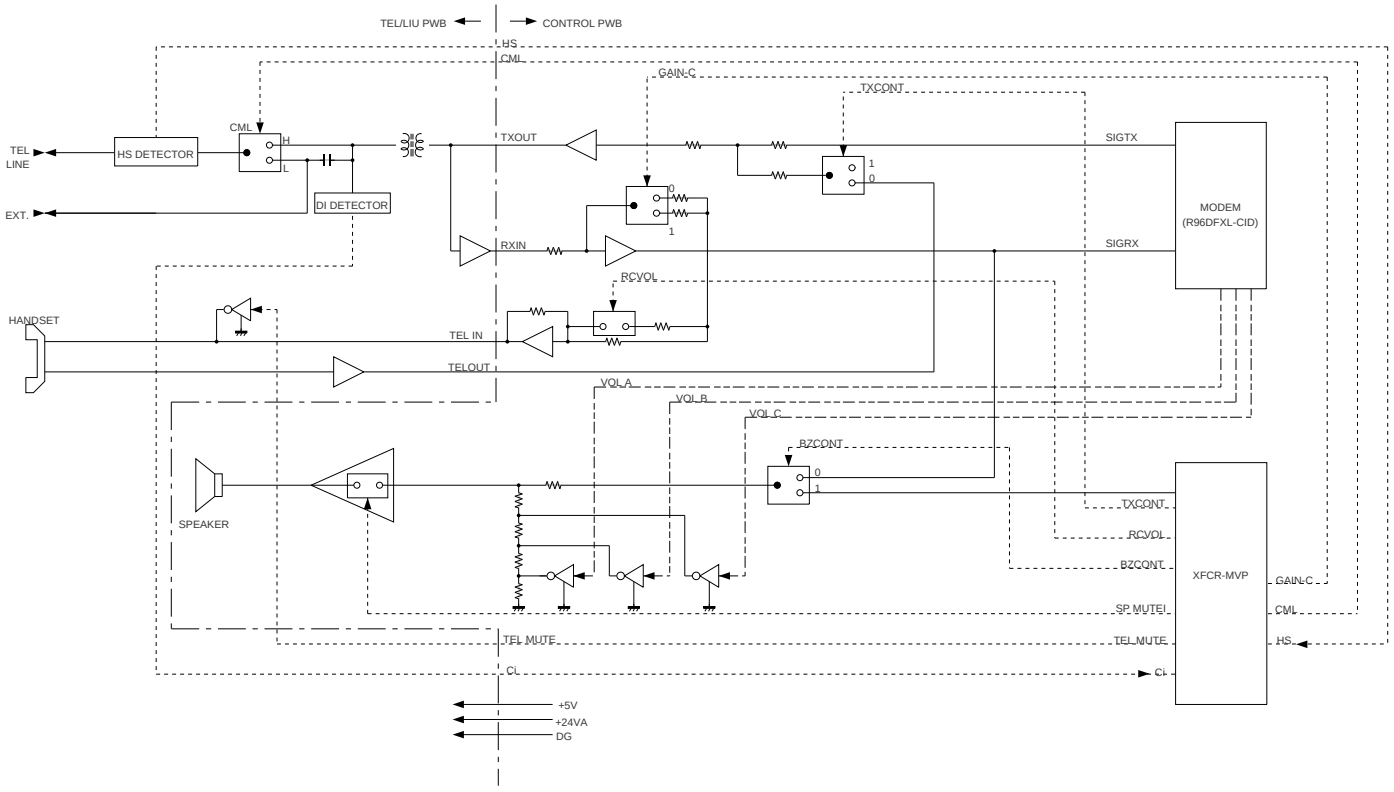

Fig. 7

[4] Circuit description of power supply PWB

1. Block diagram

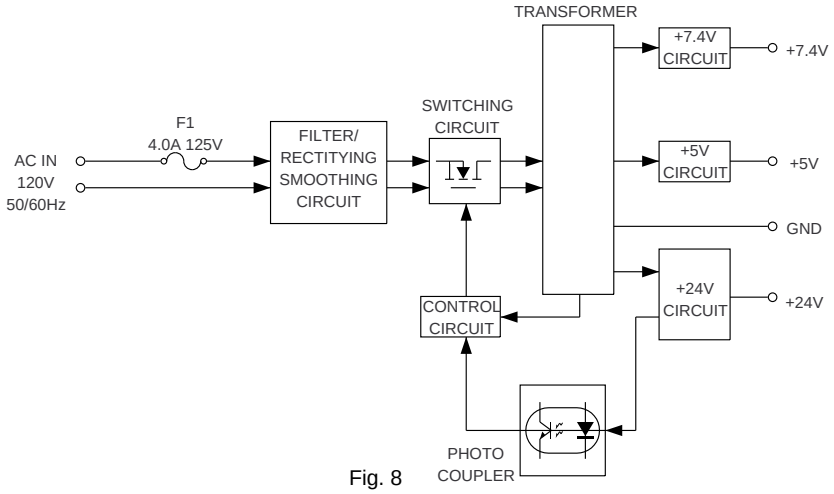

Fig. 8

The power unit intakes input of AC 120V, 50/60 Hz and supplies output of +24V, +7.4V and +5V as shown in the block diagram. (See Fig. 8.)

2-1. Filter, rectifying and smoothening circuit

In the filter section, the noise generated from the power unit is eliminated from being discharged to the external, and external noise is prevented from entering. Thunder or other excessive surge is prevented by the varistor Z1.
In the rectifying and smoothening section, AC input is rectified by the diodes D10, 11, 12 and 13, and is smoothened by the capacitor C5.
Thus, DC voltage is supplied to the switching section. Moreover, the thermistor NTC1 prevents surge current when the power is turned on.

2-2. Switching section

The circuit uses the ringing choke converter of a self-excited type.
Since MOS.
FETQ1 is repeatedly turned on and off in this system, the DC voltage supplied from the rectifying and smoothening section is converted into the high frequency pulses. While Q1 is on, energy is accumulated in the primary winding of the transformer T1, and while Q1 is off, energy is discharged to the secondary side. Thus, the power is supplied.
Moreover, the frequency is varied depending on the load of the output. As the load becomes the heavier, the frequency becomes the smaller to extend the ON period.
The constant voltage is controlled by applying the feedback to the control circuit through the photo coupler PC1 from +24V output. The overcurrent-protective circuit detects that the ON period becomes the wider as the output load becomes the heavier. For the control, the OFF period is extended by the control circuit to squeeze the energy which is accumulated in the primary winding of the transformer T1.
For protection against overvoltage, the rise of the output voltage of +24V on the secondary side is brought into the overcurrent state through the continuity of the power zener diode D104 between +24V output and GND. Thus, the overcurrent-protective circuit of the control circuit is activated for the protection.

2-3. +24V circuit

Output is supplied by rectifying and smoothening the output of the transformer T1 with the diode D101 and capacitor C101.

2-4. +5V circuit

+5 V output is generated by rectifying and smoothening the output of the transformer T1 with the diode D102 and capacitor C102 and stabilizing it with the 3-terminal regulator IC103.

2-5. +7.4V circuit

This circuit rectificats and smoothings the high-frequency pulse voltage, and output the DC +7.4V to the equipment.

[5] Circuit description of CIS PWB

The CIS board picks up optical information from the document, converts it into an electrical (analog) signal and transfers it to the control board.

(1) Block diagram

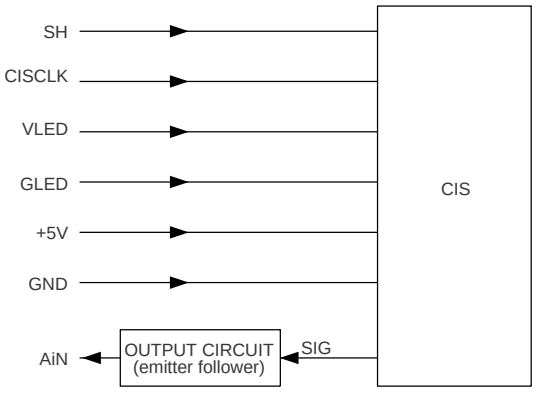

Fig. 9

(2) Description of blocks

1. CIS

The DL100-05AUJS is a highly sensitive charged coupled image sensor that consists of 2160 picture elements.

Receiving four drive signal (SI,CLK) from the control board, the tranferred photoelectric analog signal SIG is impedance converted, and the signal AiN, is supplied to the control board.

2. Waveforms

1. CLK, SI, SIG signals within the control board.

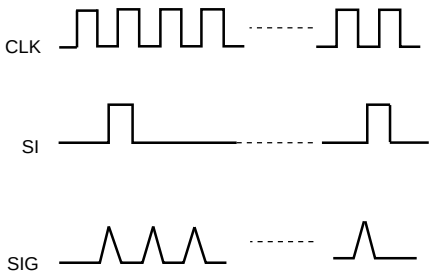

Fig. 10